Electrical Power and Energy Systems 138 (2022) 107928

Contents lists available at ScienceDirect

International Journal of Electrical Power and Energy Systems

journal homepage: www.elsevier.com/locate/ijepes

# Power-sharing for dc microgrid with composite storage devices and voltage restoration without communication

Renan F. Bastos [a], Cassius R. Aguiar [b], Attila Balogh [d], Zoltán Sütő [d,*], Ricardo Q. Machado [c]

[a] Federal University of Ouro Preto, Ouro Preto, Brazil
[b] Federal University of Technology – Paraná, Toledo, Brazil
[c] University of São Paulo, São Carlos, Brazil
[d] Department of Automation and Applied Informatics, Budapest University of Technology and Economics, Budapest, Hungary

ARTICLE INFO

*Keywords:*
DC microgrid
Power-sharing
Batteries
Ultracapacitor
DC-link voltage restoration

ABSTRACT

In this paper, we propose a new decentralized control and power-sharing strategy to manage the power flow among energy sources (ESs), energy storage systems (ESSs) and the common dc-link. In the proposed technique, we eliminate all communication among the ESSs, to reduce the complexity and increase reliability, maintaining dc-link voltage restoration. In this context, batteries and ultracapacitors (UCs) are the ESSs, while ESs can be any power source such as photovoltaic, wind, fuel-cell and etc. This technique shares the microgrid power imbalance between batteries, proportionally to their state-of-charge (SoC) and energy capacity, achieving SoC equalization. The technique also promotes voltage restoration for the UCs, keeping their average voltage constant after supplying the power peaks during power transients. For all ESSs only local variables are measured, such as local current and dc-link voltage, with no shared data between ESSs. Small signal and stability analysis are performed, along with experimental results in a lab bench show the feasibility and performance of the technique.

## 1. Introduction

The concepts of dc microgrids were introduced several years ago [1] to integrate different renewable energy sources (RESs), energy storage systems and loads. Because of the dc characteristic, all kinds of ESs and ESSs are connected to the dc-link via dc–dc power converters, i.e. this type of solution does not need a mechanism of synchronization, a methodology to control the reactive power flow, a strategy for harmonic compensation or a method of phase balancing as well.

This type of solution shows reduced level of complexity when compared to ac microgrids, at the same time the global efficiency and the power quality are increased [2–5]. In this context, the key factor in terms of management and operation of a dc microgrid is the controller interface used to manage the ESs and ESSs, which needs to ensure the stability of the dc microgrid and to provide power-sharing among the ESs and ESSs [2].

A great number of control methodologies for power-sharing in microgrids have been published in the last years [2–19], however, all of them have either some communication line between ESSs, or voltage error in the dc-link. In [2], a low-bandwidth communication (LBC) combined with a droop control method was introduced to share the power among ESSs and to achieve dc-link voltage restoration. To achieve power-sharing combined with voltage restoration, all the ESSs communicate between themselves. Moreover, the Authors also did not consider a composite storage system with batteries and ultracapacitors (UCs), but only a battery storage system to absorb the whole load transients.

In [6], the Authors apply a centralized droop strategy to manage the microgrid and to share the power among batteries, however, the technique does not include UCs as shown in [2]. A decentralized control strategy is proposed in [7–9], where the dc-link voltage deviation was used as load sharing signal, resulting in unavoidable voltage deviation in the dc-link. Furthermore, a composite energy storage system with UCs and batteries was also not considered, requiring from the storage device the total effort to supply power steps produced by the load connection as illustrated in [2].

In [10–12], the Authors considered a composite storage system, combining UCs and batteries to share the power transients and steady-state regimes. The dc-link voltage restoration was also implemented; however, these functionalities use a centralized control strategy with

* Corresponding author.
*E-mail addresses:* renan.bastos@ufop.edu.br (R.F. Bastos), cassiusaguiar@utfpr.edu.br (C.R. Aguiar), attila.balogh@aut.bme.hu (A. Balogh), zoltan.suto@aut.bme.hu (Z. Sütő), rquadros@sc.usp.br (R.Q. Machado).

https://doi.org/10.1016/j.ijepes.2021.107928
Received 15 April 2021; Received in revised form 5 July 2021; Accepted 26 December 2021
Available online 21 January 2022

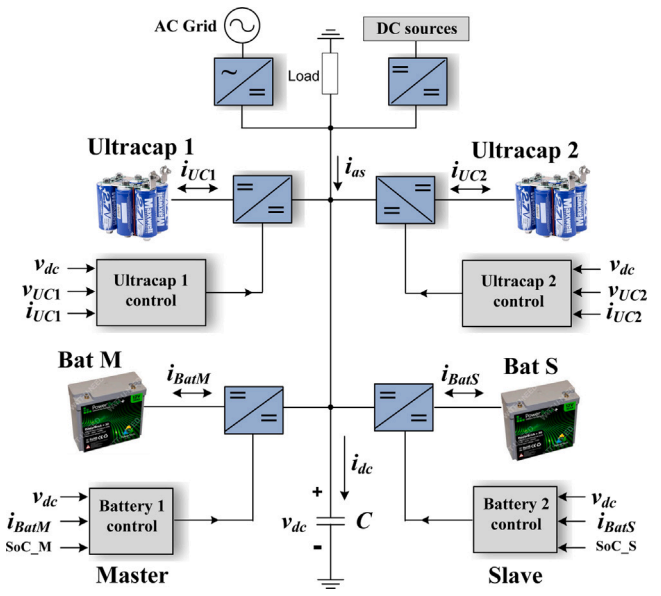


**Fig. 1.** A general circuit of a dc microgrid. Because there is no need for a communication link, the ESSs and ESs do not need to be close to each other, allowing the microgrid to be expanded in a big physical area.

a high-bandwidth communication (HBC) link between the battery controllers and UC controllers as well. In addition, neither of these papers considered the battery equalization nor the UC voltage restoration.

In [14], the concept of frequency-coordinating virtual impedance is proposed for the autonomous control of a dc microgrid. With an effective frequency-domain shaping of the virtual output impedances, the battery and UC converters are designed to absorb low-frequency and high-frequency power fluctuations, respectively.

However, despite achieving decentralized power-sharing among UC and battery, with UC voltage restoration, this paper does not discuss a scenario of multiple batteries (and equalization) or multiple UCs, nor the effect of the time constant of their filters in the dynamic or stability analysis.

Based on the aforementioned literature, we present the contributions of this paper to overcome the limitations presented in [2–19]. We propose a plug-and-play decentralized power-sharing strategy to allow multiple batteries and ultracapacitors in a composite storage system, with UC and dc-link voltage restoration, SoC equalization for batteries and no communication required between EESs. The only communication link among the ESSs is performed via physical connection over the dc-link. The battery power-sharing strategy is based on simple PI controllers with a high-pass filter (HPF) synchronization feature (combined with a SoC based equalization gain). Stability analysis is performed for many scenarios to prove the effectiveness of the proposed approach.

Because this new strategy has a plug-and-play capability, the dc microgrid can be expanded by simply adding new ESSs without the need for redesigning the controllers or even reprogramming a central controller, since the ESS control strategy is done independently of each other. This paper is organized as follows: in Section 2 the general description of the dc microgrid is presented, along with the state-space model and the analysis of the power-sharing structure. In Section 3, a mathematical analysis of the system is made, where the root locus is performed to prove the system's stability and the influence of the SoC on the stability. In Section 4, simulation results are presented, showing the performance of the proposed techniques under different circumstances. Section 5 presents the experimental results, corroborating the simulation and proving the effectiveness of proposed techniques. Finally, Section 6 presents the conclusions of the paper.

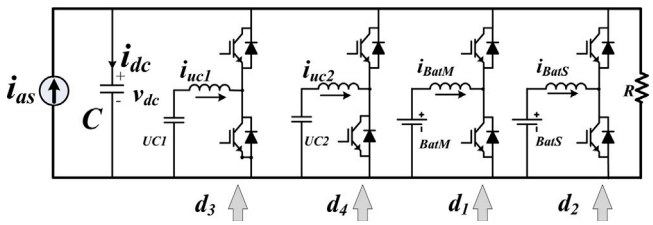


**Fig. 2.** Electrical representation of the dc microgrid.

## 2. System description, average model and proposed control technique

A general microgrid structure with the proposed ESSs control devices are depicted in Fig. 1. As it can be noticed, the ESSs do not have any communication channel between themselves, except the dc-link physical connection. All the ESSs only measure local variables, such as: the dc-link voltage ($v_{dc}$), output current ($i_{Bat}$) and estimated SoC for the batteries. For the UCs, the measured variables are the dc-link voltage, output current ($i_{UC}$) and the UC terminal voltage ($v_{UC}$). For equalization purposes, each battery estimates its own SoC by integrating the output current ($i_{Bat}$) and the UCs calculate its total energy by the terminal voltage ($v_{UC}$).

### 2.1. Microgrid state-space model

The power electronic structure from Fig. 1 can be described as Fig. 2, with four non-isolated bidirectional dc–dc converters, a dc resistive load ($R$), a dc-link capacitor ($C$) and a current source ($i_{as}$ ± depending on the power balance) to represent the ESs and Grid-tie converter. The ESSs are described as two battery packs, one defined as the Master and another as the Slave ($BatM$ and $BatS$), modeled as two independent dc sources ($V_{BatM}$ and $V_{BatS}$) and two ultracapacitor devices ($UC_1$ and $UC_2$) modeled as ideal capacitors. Additionally, the dc–dc converter's inductance is $L_{dc}$, $R_L$ for the inductance losses and $d_1, \ldots, d_4$ are the converter's duty-cycle. Each dc–dc converter can be modeled using the general operator $\delta_j = 1 - d_j$ where $j = 1, 2, 3, 4$. The complete state-space model for Fig. 2 can be represented by Eq. (1) and it will be used for the average simulation of the microgrid with the proposed control strategy (see Eq. (1) Box I).

In order to design the current controllers and perform stability analysis, each arm of the converter from Fig. 2 is represented by a generic bidirectional converter (Fig. 3). This simplification is done in order to obtain the small signal transfer function of each arm. In this representation, the ESSs are modeled as an ideal voltage sources ($V_{IN}$) with a series resistance ($R_{IN}$). Even the UCs will have the same representation, since they are very large capacitors and the control strategy will keep their average voltage constant. $C_{IN}$ is the input capacitor for the converter and the dc-link is defined as an ideal dc voltage source, based on the fact that in normal operation $v_{dc}$ will be controlled with constant average value.

Obtaining the state-space model of Fig. 3 and applying the small signal analysis, Eq. (2) can be written

$$G_C(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \\ = \frac{V_{dc}(R_{IN}C_{IN}s + 1)}{R_{IN}C_{IN}L_{dc}s^2 + (R_L R_{IN}C_{IN} + L_{dc})s + R_L + R_{IN}} \quad (2)$$

and represents the dynamic response for each dc–dc converter of the microgrid. This representation will be used to design the current controllers for all the microgrid arms.

$$\frac{d}{dt}\begin{bmatrix} i_{BatM} \\ i_{BatS} \\ i_{UC1} \\ i_{UC2} \\ v_{dc} \\ v_{UC1} \\ v_{UC2} \end{bmatrix} = \begin{bmatrix} -\frac{R_L}{L_{dc}} & 0 & 0 & 0 & -\frac{\delta_1}{L_{dc}} & 0 & 0 \\ 0 & -\frac{R_L}{L_{dc}} & 0 & 0 & -\frac{\delta_2}{L_{dc}} & 0 & 0 \\ 0 & 0 & -\frac{R_L}{L_{dc}} & 0 & -\frac{\delta_3}{L_{dc}} & \frac{1}{L_{dc}} & 0 \\ 0 & 0 & 0 & -\frac{R_L}{L_{dc}} & -\frac{\delta_4}{L_{dc}} & 0 & \frac{1}{L_{dc}} \\ \frac{\delta_1}{C} & \frac{\delta_2}{C} & \frac{\delta_3}{C} & \frac{\delta_4}{C} & -\frac{1}{RC} & 0 & 0 \\ 0 & 0 & -\frac{1}{UC_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{UC_2} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{BatM} \\ i_{BatS} \\ i_{UC1} \\ i_{UC2} \\ v_{dc} \\ v_{UC1} \\ v_{UC2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{dc}} & 0 & 0 \\ 0 & \frac{1}{L_{dc}} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{BatM} \\ v_{BatS} \\ i_{as} \end{bmatrix} \quad (1)$$

**Box I.**

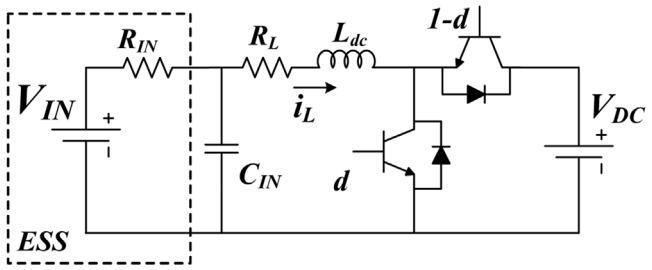


**Fig. 3.** Generic model for all ESSs converters.

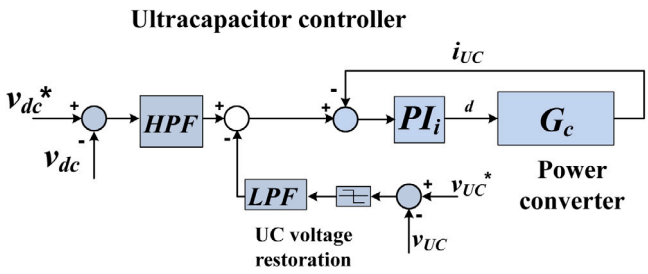


**Fig. 4.** UC control unit.

### 2.2. Proposed power-sharing

The proposed control structure for management of the UCs and batteries are depicted in Figs. 4 and 5, respectively. The goal of this technique is to share the peak transient power among the UCs with terminal voltage restoration, share the steady-state power among the batteries with SoC equalization and dc-link voltage restoration, all without communication among ESSs.

Resuming the UC control strategy (Fig. 4) in simple terms, the current reference is generated by a HPF response (Eq. (3)) on the dc-link voltage error, generating a peak current for every fast load transient.

$$\begin{cases} LPF(s) = K_b \dfrac{1}{\tau s + 1} \\ HPF(s) = K_c \dfrac{\tau s}{\tau s + 1} \end{cases} \quad (3)$$

This current peak will then create a voltage deviation in $v_{UC}$, which is restored by the UC voltage compensation branch. This compensation is made by adjusting the current reference according to the UC voltage deviation. In order for the voltage compensation not to disturb the HPF response, a low-pass filter (LPF) is applied on the voltage error, thus delaying the restoration process to act only after the HPF. For that to be effective, the time constant of both filters ($\tau$) have to be equal, or the LPF slower than the HPF.

For a microgrid with multiple UCs, the control technique applied for each of them is identical (Fig. 4), except for the gains, in case each UC has a different size. The HPF gain ($K_c$) is adjusted according to the UCs capacity, where the biggest one is $K_c = 1.0$ and the others will be defined proportionally to their size. Thus they will share the power transient peak proportionally to their energy capacity.

The battery control system (Fig. 5), when multiple batteries are used, is built with one battery defined as the master (Fig. 5(a)) and all the others are set as slaves (Fig. 5(b)). In this case, only the master

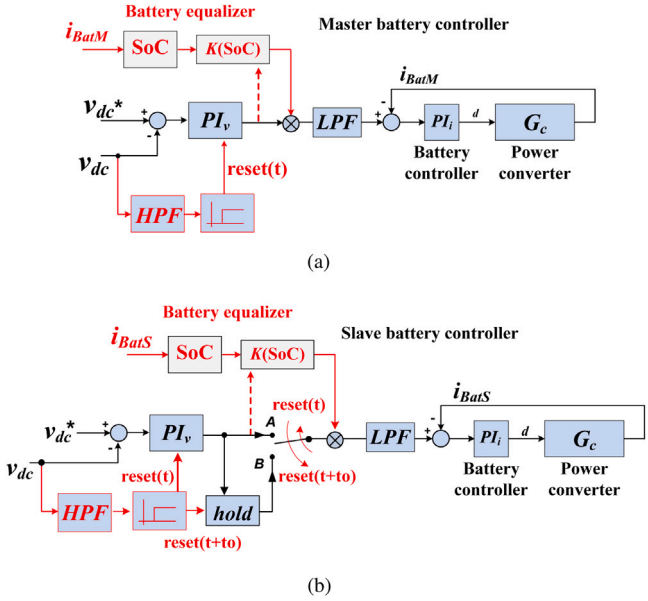


**Fig. 5.** Battery control unit. (a) Master battery controller and (b) Slave battery controller. In this technique an infinite amount of slaves can be part of the microgrid.

is responsible for the dc-link voltage integrity, while the slaves only share the load, without any stability concern.

The master battery ($BatM$) works based on a simple dc-link voltage PI controller ($PI_v$) in series with a LPF and a current PI loop ($PI_i$). In order for the batteries to equalize their SoC, a proportional gain $K(SoC)$

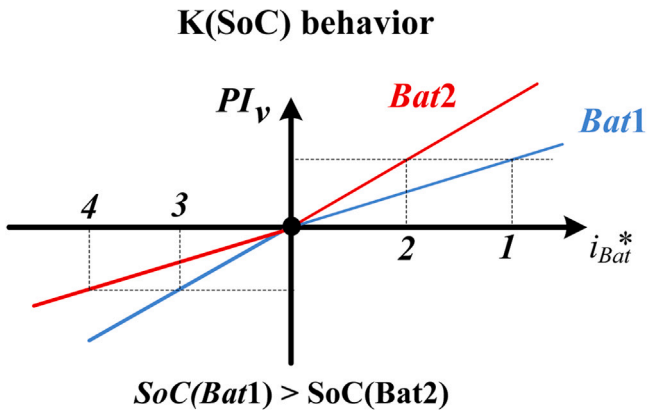


**Fig. 6.** Effect of the SoC on the battery controller, adjusting $K(SoC)$, making the battery with higher SoC to supply higher current when discharging and absorb the lowest current when charging.

adjusts the $PI_v$ output according to Eq. (4).

$$K(SoC) = \begin{cases} SoC & \text{if} \quad PI_v \geq 0 \\ 1 - SoC & \text{if} \quad PI_v < 0 \end{cases} \tag{4}$$

This gain makes the battery with higher SoC supply the highest current, when discharging, and absorbs the lowest current, when charging, leading to a point where all the SoCs and currents will be equal. The effect of $K(SoC)$ in the battery current can be illustrated by Fig. 6.

It is important to remark that is not possible to ensure full equalization for all circumstances, since there is no communications among ESSs. The only guarantee we have, is that the ESSs will always try to converge by sharing the load proportionally to their SoC, and eventually equalizing. However full equalization will depend on the behavior of the load and power generation, which are random. The only way to ensure full equalization is to include a communication layer with a central management, forcing each device to a specific setpoint for each situation. However this is not the proposition of this paper, and is a consequence for the simplicity of the technique.

The LPF has the function to make the battery current reference to change slowly during power transient and preserve the battery's life. This is possible since the UCs are responsible for the fast transient, thus the battery response can be slower. For this technique to be effective, the time constant ($\tau$) of the LPF of the battery has to be equal to the HPF of the UCs controller. The filter gain ($K_b$) can also be adjusted, when batteries have different capacities, making them to share power according to their size.

In order for the master battery to be synchronized with all the slaves, with no communication, all the $PI_v$ gains have to be identical and a reset feature is included in it (reset of the integral). The reset is performed by a HPF combined with a threshold trigger, thus every time this trigger is activated the integral of the $PI_v$ is reset. This means that at every power transient in the dc-link, the voltage controller is restarted. This feature will be further explored and better understood after the slave control is presented.

The slave battery controller is an adaptation of the master control. As it can be noticed in Fig. 5(b), the main line of the controller is identical to Fig. 5(a), with the $K(SoC)$ gain for equalization and the HPF for reset and synchronization of $PI_v$. The main difference is a selection switch between the $PI_v$ output (position A) and a $HOLD$ block output (position B), that holds the $PI_v$ value when it is triggered. In steady-state, the switch is always in the position B, with a constant current reference value from the hold block. After a random fast transient, if a reset happens (at instant $t$), the $PI_v$ is reset and the switch moves to position A, and going back to position B after $t_o$ seconds (Fig. 7). At the moment the switch goes back to position B, the hold block saves the final value of $PI_v$, keeping it until the next reset event.

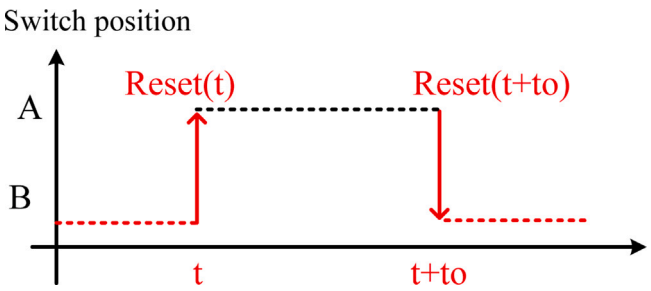


**Fig. 7.** Behavior of the switch in the slave control systems. After every fast transient, resulting in a reset signal, the switch goes to position A and back to B after $t_o$ seconds.

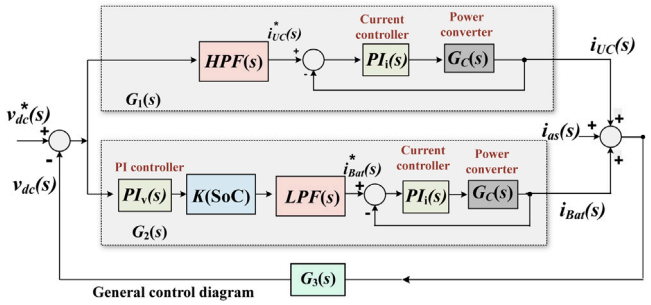


**Fig. 8.** Flow chart of the dc microgrid and control technique.

In simple terms, the slave batteries will keep a constant current delivery in steady-state, and at every power transient they use a temporary PI controller only to define the new reference. Since all batteries, master and slaves, are reset together at every transient, their $PI_v$ controllers will accumulate approximately the same value after $t_o$ (if they have the same parameters), sharing the current equally. Using the $K(SoC)$ and the LPF gain, the power share can be modulated according to SoC and battery size.

It is important to remark that the slave controller cannot stay for long time in the position A, because small differences (for long periods) between the master and the slave voltage measurements can lead to uneven sharing. The switch should stay in position A just enough time for the dc-link voltage to be recovered. Since there is no communication between the ESSs, more slave batteries can be connected in the microgrid at any time. The only procedure a new incoming battery has to perform is a fast forced current transient, in order to reset all the controllers and synchronize the master and the slaves.

## 3. Stability analysis

To analyze the stability of the proposed system, the transfer function of the microgrid from Fig. 2 is built and the root locus will be analyzed, evaluating the ESSs stability on the dc-link compensation. Additionally, we plot the behavior of the poles of the main control loop when $K(SoC)$ assumes different values, affecting the global stability.

Representing the dc microgrid in a flow chart, considering only one battery (master battery) and one UC, for stability analysis, we obtain the model in the frequency-domains as shown in Fig. 8. In the same figure, the dc–dc converters are represented by the transfer function $G_C(s)$ and its controller, $PI_i(s)$.

In Eq. (5), we represent the effect of the dc-link voltage error ($\hat{v}_{dc}(s)$) in the UC current ($\hat{i}_{UC}(s)$).

$$G_1(s) = \frac{\hat{i}_{UC}(s)}{\hat{v}_{dc}(s)} = HPF(s)\,\frac{G_C(s)\,PI_i(s)}{1 + G_C(s)\,PI_i(s)} \tag{5}$$

For this case we consider the UC terminal voltage constant, so we neglect the UC voltage restoration branch. The effect of the dc-link

**Table 1**
System parameters.

| Parameter | Symbol | Value |
|---|---|---|
| ESS equivalent model voltage | $v_{EQ}$ | 80 V |
| dc-link voltage reference | $V^*_{dc}$ | 250 V |
| UC voltage reference | $V^*_{UC}$ | 85 V |
| dc–dc converter input capacitance | $C_{IN}$ | 1000 μF |
| dc–dc converter inductance | $L_{dc}$ | 3 mH |
| Microgrid load | $R$ | 70 Ω |
| ESSs equivalent model resistance | $R_{IN}$ | 0.01 Ω |
| Resistance of the inductance | $R_L$ | 0.1 Ω |
| $PI_v$ proportional gain | $P_v$ | 2 |
| $PI_v$ integral gain | $I_v$ | 2 |
| $PI_i$ proportional gain | $P_i$ | 0.01 |
| $PI_i$ integral gain | $I_i$ | 1 |
| $HPF$ gain | $K_c$ | 1 |
| $LPF$ gain | $K_b$ | 1 |
| $LPF$ and $HPF$ time constants | $\tau$ | 0.05 s |
| Equalization gain | $K(SoC)$ | 0.5 |
| Reset timer | $t_o$ | 200 ms |

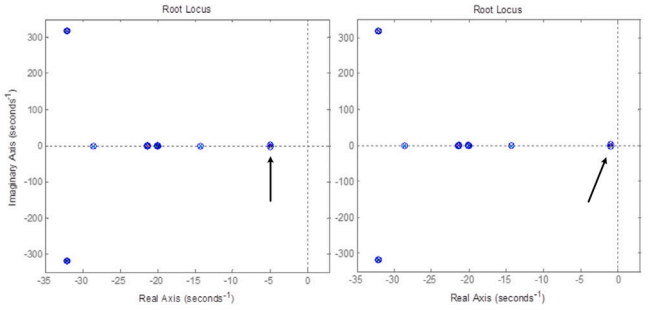


**Fig. 9.** Root locus of $G_m(s)\big|_{\hat{i}_{as}(s)=0}$ for $K(SoC) = 0.5$ and $K(SoC) = 0.1$, respectively. This shows that the lower is $K(SoC)$, less stable is the system, since the highlighted pole moves to the right when the gain is reduced.

voltage error in the battery current ($\hat{i}_{Bat}(s)$) can be represented by Eq. (6).

$$G_2(s) = \frac{\hat{i}_{Bat}(s)}{\hat{v}_{dc}(s)} = PI_v(s)\,K(SoC)\,LPF(s)\,\frac{G_C(s)\,PI_i(s)}{1 + G_C(s)\,PI_i(s)} \tag{6}$$

Finally, the dc-link with its resistive load can be represented by Eq. (7).

$$G_3(s) = \frac{\hat{v}_{dc}(s)}{\hat{i}(s)} = \frac{R}{RCs + 1} \tag{7}$$

Combining these sub-systems, as in Fig. 8, we have a simplified representation for the microgrid as Eq. (8).

$$G_m(s)\Big|_{\hat{i}_{as}(s)=0} = \frac{(G_1(s) + G_2(s))G_3(s)}{1 + (G_1(s) + G_2(s))G_3(s)} \tag{8}$$

The parameters used for the root locus are presented in Table 1 and are applied in Eq. (5) to (8) for two different values of $K(SoC)$.

The result from Fig. 9 gives a very interesting conclusion: the smaller is the $K(SoC)$ gain for the master controller, less stable the microgrid becomes. Since this gain is adjusted automatically according to the SoC of the master (Eq. (4)), the technique has to limit this gain, avoiding low values to prevent instability. This result is obvious if we consider that the gain $K(SoC)$ modulates the $PI_v$ output, thus if the gain is small, then the $PI_v$ action reduces, resulting in less stability. As a consequence, in practice, the master battery must have a SoC equalization band zone, with a higher and lower limit, when out of that, the equalization feature is disabled. For the slave batteries, this feature has no consequence for the stability of the microgrid, since only the master is the responsible for the dc-link voltage integrity.

As mentioned before, the time constant of the LPF of the batteries, the HPF and LPF of the UC must have the same value in order to work with harmony. These filters work to preserve the batteries from fast

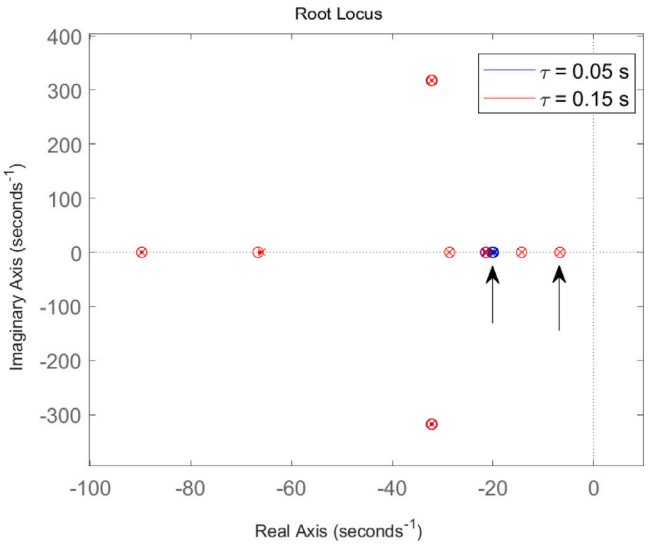


**Fig. 10.** Root locus of $G_m(s)$ for $K(SoC) = 1$ and $\tau$ changing from $\tau = 0.05$ s to $\tau = 0.15$ s. As consequence some poles move to the right, reducing the stability of the system.

**Table 2**
Simulation parameters.

| Parameter | Symbol | Value |
|---|---|---|
| Battery voltage | $V_{BatM}$, $V_{BatS}$ | 75 V |
| Ultracapacitor 1 | $UC_1$ | 0.2 F |
| Ultracapacitor 2 | $UC_2$ | 0.1 F |
| dc-link capacitor | $C$ | 1000 μF |

current transients, transferring them to the UCs. Low $\tau$ means fasts transients, bigger $\tau$ slower transients, sparing more the batteries. Using Eq. (8) for $K(SoC) = 1$ and changing the time-constant of the filters from $\tau = 0.05$ s to $\tau = 0.15$ s, we can also analyze the influence of $\tau$ in the stability of the system. From Fig. 10 it can be seen that when $\tau$ is increased, some poles move to the right, reducing the stability of the system. This means that, the slower the battery transient is made, less stable is the system. However, since $\tau$ is fixed during the operation of the system, its value can be chosen to have a good overall stability. We advise $\tau$ in the range of some milliseconds, for good stability, and providing enough current damping for the batteries.

## 4. Simulation results

In this section, average simulations using Eq. (1) are performed in order to validate the proposed techniques from Figs. 4 and 5. The controllers and converters are set with the same data from Table 1 and the EESs are built as Table 2.

The connection of a slave battery into the microgrid can be seen in Fig. 11. In order to be connected, the slave battery has to create a power transient (current step), resulting in a reset in all the $PI_v$ controller of the grid, synchronizing all ESSs. If the master and the slave batteries have the same constant SoC, they share the current equally, as in Fig. 11.

From Fig. 11 it can also be noticed that the two UCs share the power peak proportionally to their capacitances ($UC_1$ is double size of $UC_2$). This is performed by adjusting the $HPF$ gain as $K_{c1} = 1$ and $K_{c2} = 0.5$ for $UC_1$ and $UC_2$, respectively. The dc-link voltage and UC terminal voltage are restored to 250 V and 85 V respectively, as expected.

The equalization procedure can be seen in Fig. 12, where the SoC was modeled by integrating the battery current. The capacity of the batteries was defined very low, in order to achieve equalization in a few seconds. As it can be seen, for different SoCs, the batteries share

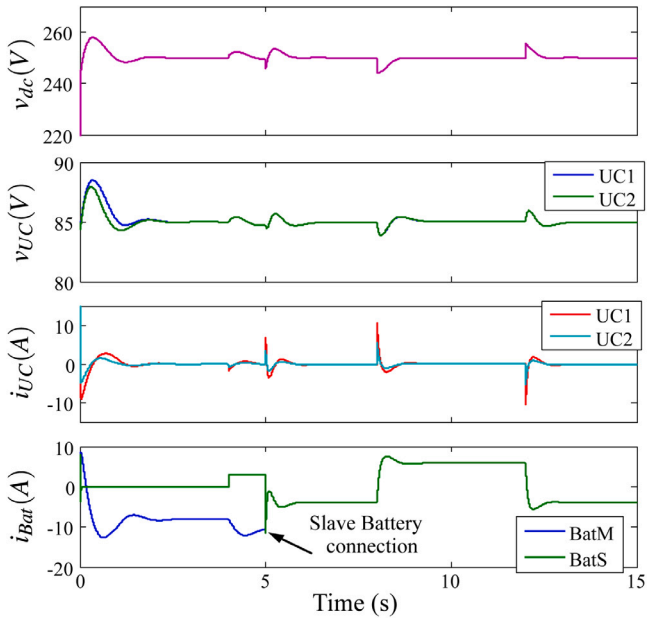


**Fig. 11.** Average simulation using Eq. (1) and the proposed control technique from Figs. 4 and 5. The slave battery is connected to the system at 5 s by creating a current transient. At 8 s and 12 s $i_{as}$ changes in step, from 6 A to 0 A and back to 6 A. In this case both batteries have the same constant SoC, sharing the load equally.

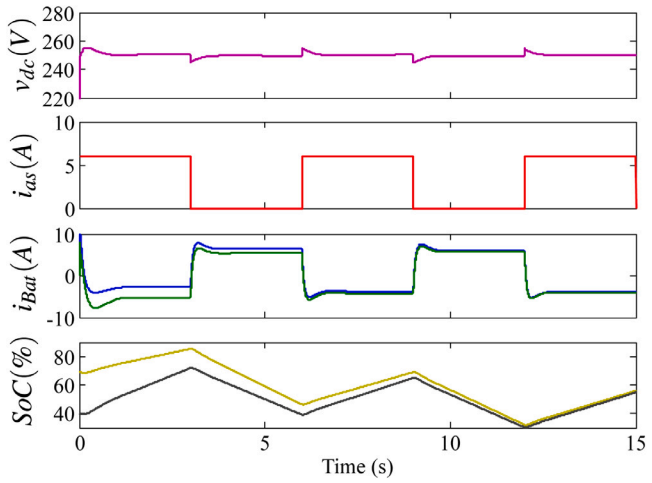


**Fig. 12.** Average simulation considering variable SoC. After some cycles of charge and discharge the master battery equalizes with the slave, sharing equally the load.

the current proportionally and after some charge and discharge cycles, their energy level equalizes, as proposed.

These simulation results show that the proposed goals are achieved, sharing peak power between UCs, steady-state power between batteries with battery equalization, UC and dc-link voltage restoration, using no communication line between EESs.

## 5. Experimental results

In this section the experimental results are performed in order to prove the effectiveness of the proposed strategies in a real scenario. Fig. 13 shows the experimental setup built according to Fig. 2, with the same parameters as the simulations, Tables 1 and 2, except for the UCs that both are identical 0.1 F. Each ESS is controlled by a separate processor (32-bit SAM3X8E ARM Cortex-M3) with no communication between them.

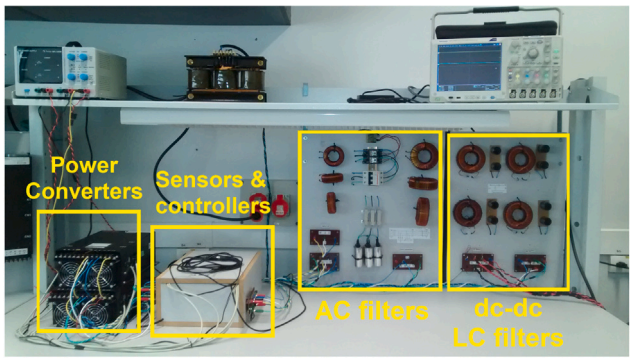


**Fig. 13.** Experimental setup.

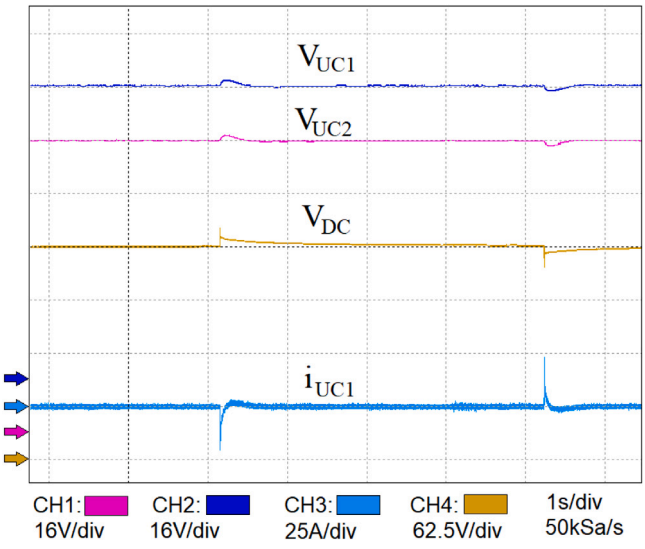


**Fig. 14.** Experimental result, $V_{UC1}$, $V_{UC2}$, $V_{DC}$ and $i_{UC1}$ respectively, during transient generated by the $i_{as}$. The UC reacts at every transient by generating a peak current and the voltage deviation is restored after every burst to 85 V. The dc-link voltage is also restored to 250 V after every transient.

The transient behavior of the UCs and dc-link can be seen in Fig. 14, when subjected to $i_{as}$ steps. As expected, their terminal voltages are being restored to their original state ($V^*_{UC} = 85$ V and $V^*_{DC} = 250$ V) after every power transient. The UCs also supply the peak transient current required at every power step in $i_{as}$.

The UC voltage reference ($V^*_{UC}$) is defined according to the maximum voltage gain of the DC–DC interface converter. In this case it was chosen to be 3× smaller than the DC-link voltage, but it could be any value from 250 V > $V^*_{UC}$ > 85 V or 1× < gain < 3×. If another DC–DC converter topology is used, this range can be reevaluated to the gain range of the chosen converter. The stability of the system is affected only by the dynamic of the interface DC–DC converter and is not affected by the chosen UC steady state voltage.

In order to include any extra battery into the microgrid, a simple procedure should be followed: the new slave should create a power transient, resetting all the controllers and synchronizing the ESSs. Fig. 15 shows exactly this procedure, when $i_{BatS}$ goes from 0 A to 20 A and back to 0 A. After this step is over, the slave battery is synchronized with master, sharing equally the current, because they have the same SoC.

As discussed in the previous sessions, the time-constant of the LPF and HPF have the function to spare the batteries of fast current transitions. Fig. 16 depicts the behavior of the UCs under power transients in the microgrid, when $\tau$ is changed from $\tau = 0.05$ s to $\tau = 0.15$ s. As it

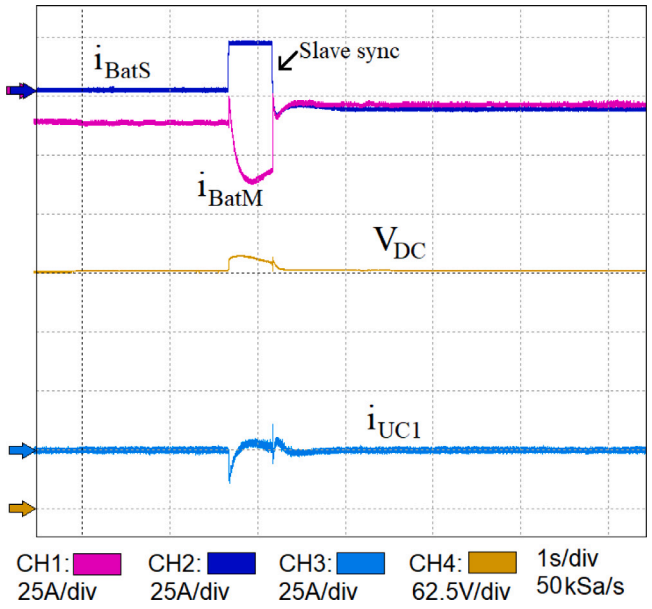


**Fig. 15.** Experimental result, $i_{BatS}$, $i_{BatM}$, $V_{DC}$ and $i_{UC1}$ respectively. In order to be connected to the system, the slave battery creates a voltage transient in the dc-link using a current step. Thus resulting in a reset and synchronization of the controllers, master and slave. After the reset the batteries deliver the same current because they have the same SoC.

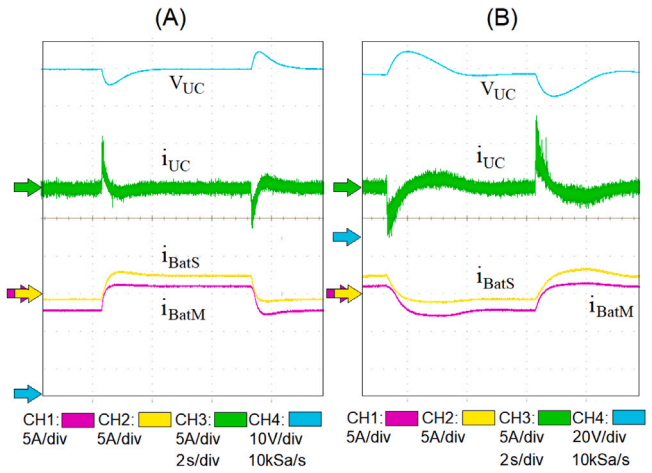


**Fig. 16.** Dynamic behavior when time-constant of the filters are increased from $\tau = 0.05\,s$ (A) to $\tau = 0.15\,s$ (B). All the transients become slower and the voltage deviation of the UC increases, but it is restored right after to the intended value of 85 V. In this case $SoC_{BatM} = 0.4$ and $SoC_{BatS} = 0.7$ creating a proportional sharing.

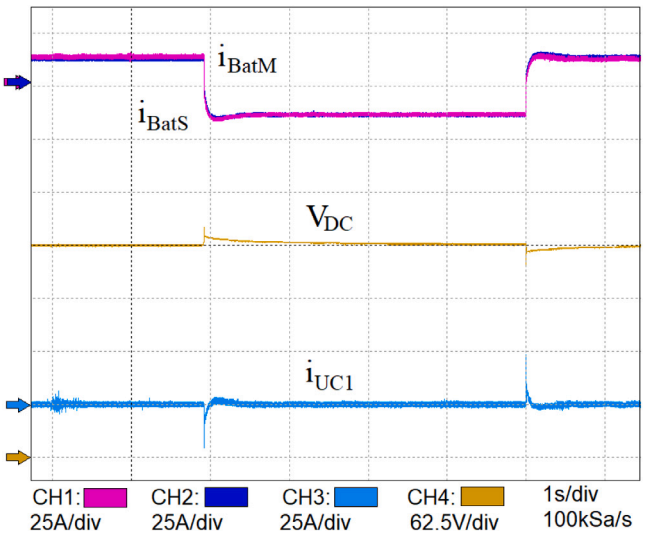


**Fig. 17.** Experimental result, $i_{BatS}$, $i_{BatM}$, $V_{DC}$ and $i_{UC1}$ respectively. Batteries supplying steady state regime power and UCs the transient power. After synchronization, in every power transient the batteries share the transient equally, because their SoC is the same.

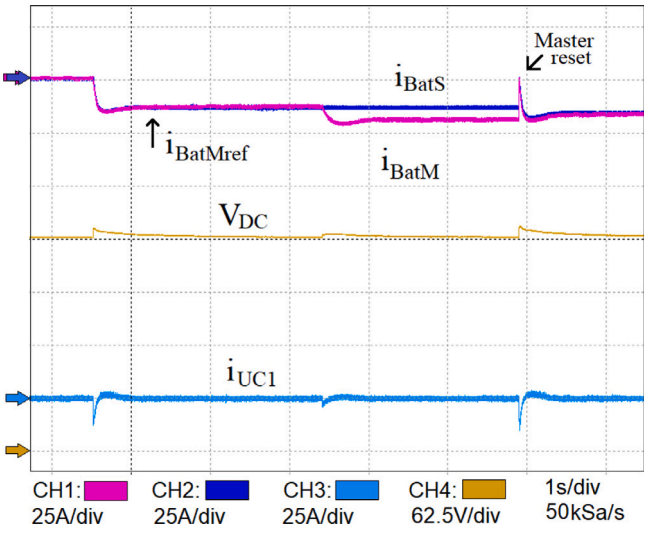


**Fig. 18.** Experimental result, $i_{BatS}$, $i_{BatM}$, $V_{DC}$ and $i_{UC1}$ respectively. If the master battery have a change in the delivered current, created by $i_{as}$, without detecting any reset in the system, it will automatically create a disturbance and force a synchronization reset, to recover the power share.

can be seen, when the constant is increased, the current transients of UCs and batteries become slower, sparing the batteries from fast current change and creating bigger voltage deviations in $V_{UC}$. This shows how the time-constant performance is an important role in the behavior of the system, however it was shown in the previous session that, bigger $\tau$, results in less stability.

The normal operation behavior of the master and the slave after the synchronization is depicted in Fig. 17. As expected, the batteries share the steady-state power and the UCs the fast transient, restoring the UCs and dc-link voltages. As proposed, it was not necessary to exchange any data between the ESSs to achieve these results, thanks to the proposed technique.

In case a smooth power transient is created by $i_{as}$, not strong enough to trigger the reset feature from the technique (Fig. 5), the slave battery will not take to itself any share of the extra power. Thus, the master battery has to deal with all the extra energy alone, creating a sharing error between master and slave. In order to solve this sharing error, the master battery will always analyze its power deliver using a threshold limit (defined by the operator). Thus, after every synchronization reset, the master battery will save the current deliver value ($i_{BatMref}$) and keep comparing it to the instantaneous deliver.

If the threshold limit is hit, before a reset, means that there is sharing deviation. Then, the master battery will create a power transient, synchronizing again all the ESSs. Fig. 18 shows this procedure being performed, equalizing the master and slave after an uneven sharing. This method ensures that even if there would be a power-sharing unbalance, it will not be too big. The size of this deviation is up to the operator, since the threshold is adjustable. However, the smaller the limit is; more reset events will be triggered during operation.

As it was proposed, the technique is plug-and-play, with the possibility to integrate more EESs at any time. Fig. 19 depicts the microgrid with three batteries and one UC, where we have one master and two

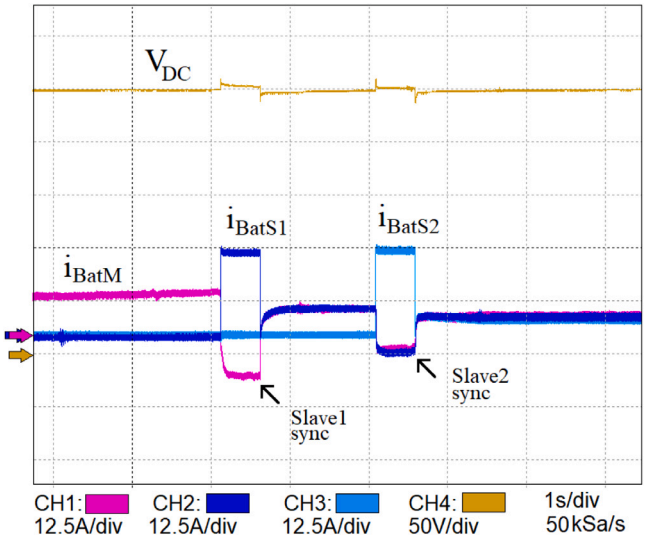


**Fig. 19.** Experimental result, $V_{DC}$, $i_{BatM}$, $i_{BatS1}$ and $i_{BatS2}$, respectively. Initially only the master battery is connected, and then a first slave battery is connected, sharing the load with the master. After some time, a second slave battery is connected, sharing the load with the master and the Slave1. For this example, all three batteries have the same SoC.

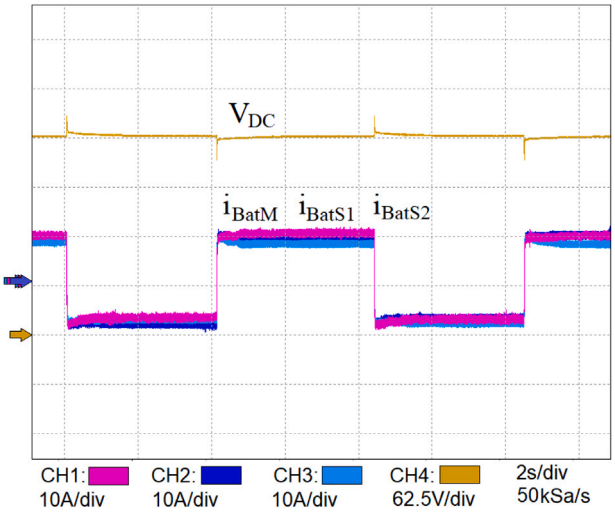


**Fig. 20.** Experimental result, $V_{DC}$, $i_{BatM}$, $i_{BatS1}$ and $i_{BatS2}$, respectively. The master battery sharing the load with the two slaves equally during power transients in $i_{as}$. All three have the same SoC.

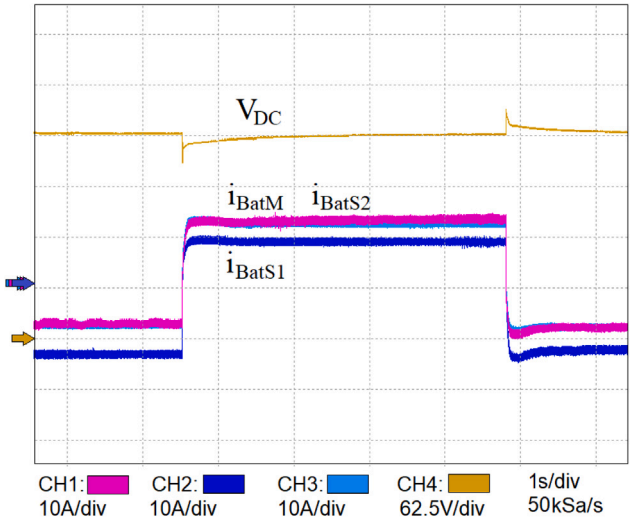


**Fig. 21.** Experimental result, $V_{DC}$, $i_{BatM}$, $i_{BatS1}$ and $i_{BatS2}$, respectively. In this case $SoC_{BatM} = 0.5$, $SoC_{BatS1} = 0.3$ and $SoC_{BatS2} = 0.5$, resulting in the master and the Slave2 to share the same current, with Slave1 with a smaller current delivery.

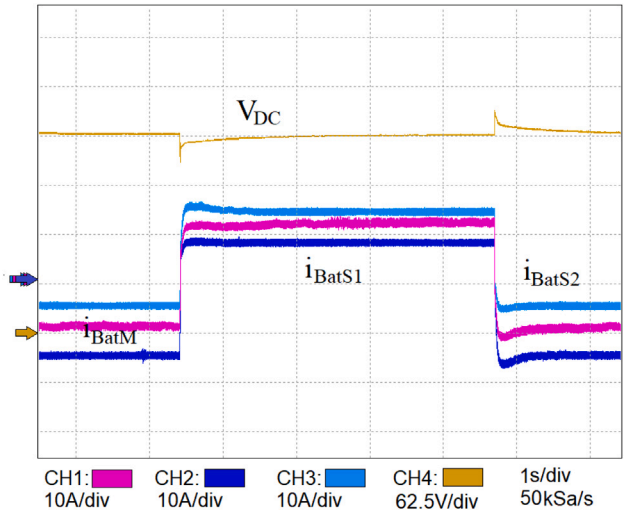


**Fig. 22.** Experimental result, $V_{DC}$, $i_{BatM}$, $i_{BatS1}$ and $i_{BatS2}$, respectively. In this case $SoC_{BatM} = 0.5$, $SoC_{BatS1} = 0.3$ and $SoC_{BatS2} = 0.7$, resulting in a power deliver proportional to their SoC.

slave batteries connected. For multiple batteries the procedure is the same as in Fig. 15, every new incoming battery should create a power transient, synchronizing with the master and the other slaves in the system. In Fig. 19, the Slave1 is the first to be connected, sharing equally the load with the master after the reset. After some time, the Slave2 repeats the connection procedure, sharing the total load equally with the master and the Slave1.

Since the master, Slave1 and Slave2 have the same SoC, they share the same current after all synchronization, as in Fig. 20, showing the behavior of the three ESSs during power transients created by $i_{as}$. If the ESSs have different SoC, the technique will ensure proportional sharing according to Eq. (4), as in Figs. 21 and 22.

The power-sharing if the master has a $SoC_{BatM} = 0.5$, the Slave1 a $SoC_{BatS1} = 0.3$ and the Slave2 $SoC_{BatS2} = 0.5$ is depicted in Fig. 21. If the master has a $SoC_{BatM} = 0.5$, the Slave1 a $SoC_{BatS1} = 0.3$ and the Slave2 $SoC_{BatS2} = 0.7$ is depicted in Fig. 22. In both cases, it is clear that the proposed technique behaves as expected, sharing the load according to the SoC with dc-link voltage restoration ($V_{dc}^{*} = 250$ V) even though the ESSs are not using any communication channel among them.

## 6. Conclusions

In this paper a decentralized control strategy was proposed in order to manage the power-sharing between EESs without communication among the storage devices. In this strategy, the batteries are responsible for supplying/absorbing the steady-state power transients and UC the fast power transient, achieving UC and dc-link voltage restoration and battery equalization. In addition, the proposed strategy presents plug-and-play capability, without requiring any control redesign in case of system expansion, increasing the system reliability and versatility.

A stability analysis was made; and it was shown that it is affected by $K(SoC)$ on the master battery. Thus, this gain has to be limited in order to keep the system stable. The average simulation showed a high degree of precision, since all the results obtained in the simulator were observed in the experimental bench.

The lab results show that the proposed technique is a very simple and powerful way of integration for ESSs into a microgrid. Seeing that it uses simple PI controllers with some very straightforward adaptations and does not require a communication channel among ESSs. A big advantage compared to other proposed techniques in the literature, where most of them use very complex mathematical functions or very complex control structures, combined with a communication link in some cases. The lab results also showed how effective the proposed technique is in integrating several ESSs in a plug-and-play operation, where batteries were inserted in to the microgrid on the fly.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Acknowledgments

The research reported in this paper and carried out at the Budapest University of Technology and Economics has been supported by the National Research Development and Innovation Fund based on the charter of bolster issued by the National Research Development and Innovation Office under the auspices of the Ministry for Innovation and Technology, Hungary.

## References

[1] Lasseter R, Akhil A, Marnay C, Stephens J, Dagle J, Guttromsom R, et al. Integration of Distributed Energy Resources. The CERTS Microgrid Concept. Tech. Rep. LBNL–50829, U.S. Department of Energy; 2002, p. 799644. http://dx.doi.org/10.2172/799644.

[2] Lu X, Guerrero JM, Sun K, Vasquez JC. An improved droop control method for DC microgrids based on low bandwidth communication with DC bus voltage restoration and enhanced current sharing accuracy. IEEE Trans. Power Electron. 2014;29(4):1800–12. http://dx.doi.org/10.1109/TPEL.2013.2266419.

[3] Xu L, Chen D. Control and operation of a DC microgrid with variable generation and energy storage. IEEE Trans. Power Deliv. 2011;26(4):2513–22. http://dx.doi.org/10.1109/TPWRD.2011.2158456.

[4] Dragičević T, Lu X, Vasquez JC, Guerrero JM. DC microgrids—Part I: A review of control strategies and stabilization techniques. IEEE Trans. Power Electron. 2016;31(7):4876–91. http://dx.doi.org/10.1109/TPEL.2015.2478859.

[5] Dragičević T, Lu X, Vasquez JC, Guerrero JM. DC microgrids—Part II: A review of power architectures, applications, and standardization issues. IEEE Trans. Power Electron. 2016;31(5):3528–49. http://dx.doi.org/10.1109/TPEL.2015.2464277.

[6] Dragičević T, Guerrero JM, Vasquez JC, Škrlec D. Supervisory control of an adaptive-droop regulated DC microgrid with battery management capability. IEEE Trans. Power Electron. 2014;29(2):695–706. http://dx.doi.org/10.1109/TPEL.2013.2257857.

[7] Sun K, Zhang L, Xing Y, Guerrero JM. A distributed control strategy based on DC bus signaling for modular photovoltaic generation systems with battery energy storage. IEEE Trans. Power Electron. 2011;26(10):3032–45. http://dx.doi.org/10.1109/TPEL.2011.2127488.

[8] Gu Y, Xiang X, Li W, He X. Mode-adaptive decentralized control for renewable DC microgrid with enhanced reliability and flexibility. IEEE Trans. Power Electron. 2014;29(9):5072–80. http://dx.doi.org/10.1109/TPEL.2013.2294204.

[9] Dragičević T, Guerrero JM, Vasquez JC. A distributed control strategy for coordination of an autonomous LVDC microgrid based on power-line signaling. IEEE Trans. Ind. Electron. 2014;61(7):3313–26. http://dx.doi.org/10.1109/TIE.2013.2282597.

[10] Tummuru NR, Mishra MK, Srinivas S. Dynamic energy management of renewable grid integrated hybrid energy storage system. IEEE Trans. Ind. Electron. 2015;62(12):7728–37. http://dx.doi.org/10.1109/TIE.2015.2455063.

[11] Zhou H, Bhattacharya T, Tran D, Siew TST, Khambadkone AM. Composite energy storage system involving battery and ultracapacitor with dynamic energy management in microgrid applications. IEEE Trans. Power Electron. 2011;26(3):923–30. http://dx.doi.org/10.1109/TPEL.2010.2095040.

[12] Li W, Xu C, Yu H, Gu Y, He X. Energy management with dual droop plus frequency dividing coordinated control strategy for electric vehicle applications. J. Mod. Power Syst. Clean Energy 2015;3(2):212–20. http://dx.doi.org/10.1007/s40565-015-0123-1.

[13] Bastos RF, Dragicevic T, Guerrero JM, Machado RQ. Decentralized control for renewable DC microgrid with composite energy storage system and UC voltage restoration connected to the grid. In: IECON 2016 - 42nd annual conference of the IEEE industrial electronics society. Florence, Italy: IEEE; 2016, p. 2016–21. http://dx.doi.org/10.1109/IECON.2016.7793249.

[14] Gu Y, Li W, He X. Frequency-coordinating virtual impedance for autonomous power management of DC microgrid. IEEE Trans. Power Electron. 2015;30(4):2328–37. http://dx.doi.org/10.1109/TPEL.2014.2325856.

[15] Han Y, Ning X, Yang P, Xu L. Review of power sharing, voltage restoration and stabilization techniques in hierarchical controlled DC microgrids. IEEE Access 2019;7:149202–23. http://dx.doi.org/10.1109/ACCESS.2019.2946706.

[16] Xia Y, Wei W, Yu M, Wang X, Peng Y. Power management for a hybrid AC/DC Microgrid With Multiple Subgrids. IEEE Trans. Power Electron. 2018;33(4):3520–33. http://dx.doi.org/10.1109/TPEL.2017.2705133.

[17] Hou N, Li Y. Communication-free power management strategy for the multiple DAB-based energy storage system in islanded DC microgrid. IEEE Trans. Power Electron. 2021;36(4):4828–38. http://dx.doi.org/10.1109/TPEL.2020.3019761.

[18] Kirakosyan A, El-Saadany EF, Moursi MSE, Yazdavar AH, Al-Durra A. Communication-free current sharing control strategy for DC microgrids and its application for AC/DC Hybrid Microgrids. IEEE Trans. Power Syst. 2020;35(1):140–51. http://dx.doi.org/10.1109/TPWRS.2019.2925779.

[19] Li X, Guo L, Li Y, Hong C, Zhang Y, Guo Z, et al. Flexible interlinking and coordinated power control of multiple DC microgrids clusters. IEEE Trans Sustain Energy 2018;9(2):904–15. http://dx.doi.org/10.1109/TSTE.2017.2765681.